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INVITED PAPER *Special Section on Progress & Trend of Superconductor-based Computers*

Toward Realization of Scalable Packaging and Wiring for Large-Scale Superconducting Quantum Computers

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SUMMARY In this paper, we review the basic components of superconducting quantum computers. We mainly focus on the packaging and wiring technologies required to realize large-scalable superconducting quantum computers.

key words: *superconducting qubit, sample packaging, three-dimensional wiring*

1. Introduction

Superconducting quantum circuits are a promising platform for realizing large-scale quantum computers. Although solid-state qubits suffer from various kinds of decoherence, continuous efforts in the last two decades both from material and design sides have improved the performance of superconducting qubits. The coherence time of the state-of-the-art superconducting qubits has reached more than 100 μs even in multi-qubit devices [1]. The fidelity of a two-qubit gate is now beyond 99% [2], and the integration of multiple qubits has attracted increasing attention to achieve higher computational functionalities. The number of qubits in superconducting devices has been scaling up rapidly, and several groups have operated 10–100-qubit processors [3]–[7].

One of the latest significant achievements in multi-qubit processors is the so-called quantum computational supremacy demonstrated by Google [3]. Their result showed the advantage of quantum computers over conventional supercomputers in a specific computational task. However, it has not directly led to an acceleration of any practical computation by the quantum computer. We are still in the early stage of building a quantum computer with error resilience in its operation to run essential algorithms like factoring [8] and database search [9]. Quantum error correction makes such fault-tolerant computation possible in a quantum computer [10]. The most promising candidate of quantum error-correcting codes for solid-state devices is the surface code [11], [12]. It only requires nearest neighbor interaction in a two-dimensional array of qubits, while it has a relatively high error threshold of $\sim$ 0.1% [13]. A next milestone toward realizing quantum computers could be demonstrating error reduction in a logical qubit encoded by a small-distance surface code [14]. Recently, an exponential suppression of the error rate with one-dimensional repetition codes has been demonstrated [15], but the gate and measurement errors are still a little bit higher than the requirement for the surface code.

As the surface code requires a two-dimensional array of qubits on a plane, superconducting quantum computers should have scalability in lateral directions. While it is straightforward to extend the circuit pattern to have a two-dimensional array of qubits, the necessity of individual control and readout of qubits makes the wiring difficult. The conventional wire bonding from the edges of the chip does not scale well to address the interior qubits in a large chip. We need to develop a way of wiring to address all of the qubits while keeping the lateral scalability.

In this paper, we review the required structure of quantum computing processors from the viewpoints of packaging and wiring. It is essential to make the overall module of the superconducting circuits scalable toward realizing large-scale superconducting quantum computers.

2. Superconducting Qubits

One of the distinguished features of superconducting circuits is that we can engineer the qubit properties by designing macroscopic circuit parameters [16]. Among various types of superconducting qubits, transmons [17] are most commonly used for integration purposes. Figure 1 shows a schematic layout and a circuit diagram of a transmon qubit. The transmon qubit is composed of a Josephson junction placed in between two large superconducting electrodes. The larger shunt capacitance makes the transmon more insensitive to charge noise, although it makes the upper limit of the speed of the gate operation slower due to the smaller qubit anharmonicity. The geometric shape of the shunt capacitor can be arbitrary, while the capacitance value is chosen to balance the coherence and connectivity of the qubit.

Recalling that the temperature-to-frequency conversion factor h/k_B is $\sim$ 50 mK/GHz, the frequency of transmon qubits should be higher than a few GHz to neglect the thermal population of qubits at the base temperature of 10–20 mK in a dilution refrigerator. Here h and k_B are the Planck and Boltzmann constants, respectively. While the superconducting gap energy of the metal in use sets the ul-

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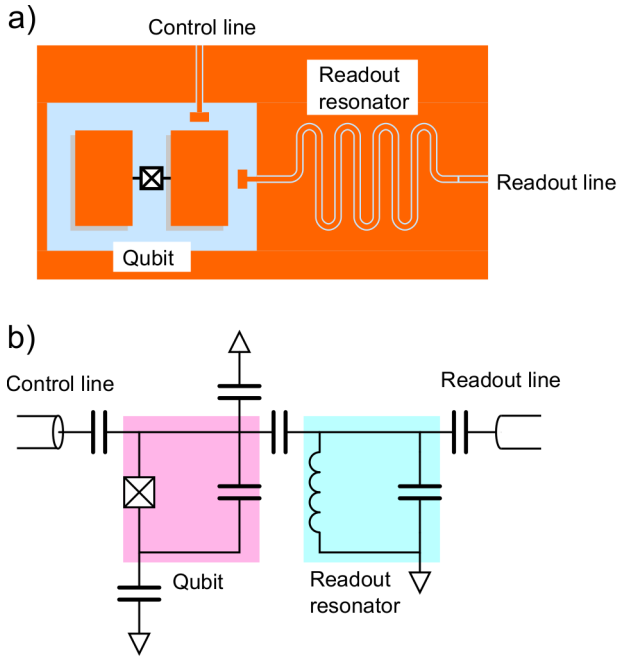

Fig. 1 (a) Circuit layout of a transmon qubit and a readout resonator. The control and readout lines are implemented with coplanar waveguides. They are capacitively coupled to the qubit and the readout resonator, respectively. An Al/AlO$_x$/Al Josephson junction (depicted as a square with a cross) is commonly used as a nonlinear inductor. (b) Equivalent circuit diagram of the transmon qubit and readout resonator.

timate upper limit of the qubit frequency, the operating frequency is usually chosen in the range of 2–10 GHz because of the broader availability of control electronics.

We manipulate the quantum state of the transmon by applying a microwave signal on resonance with the qubit frequency. A coplanar waveguide is capacitively coupled to the qubit for guiding the control signal. The readout resonator is a peripheral circuit coupled with the qubit, which is used for the dispersive readout of the qubit state. We measure a frequency shift of the readout resonator, in which the qubit state is reflected, and we infer the qubit state in a nondestructive manner [18], [19]. In the circuit layout, a superconducting qubit demands at least one control line and one readout line for each qubit. No additional controlling line is required in the architecture based on microwave-driven two-qubit gates between fixed-frequency transmons [20]. In the case of control-phase gates for flux-tunable transmons, additional dc wires for flux tuning are required for each qubit [21]. The number of readout lines can be minimized using frequency multiplexing.

The overall wiring in the dilution refrigerator is shown schematically in Fig. 2(a). The control and readout signals for qubits are generated by control electronics placed at room temperature. The microwave signals are transmitted through all the temperature stages in the refrigerator. Coaxial cables are usually employed for the wiring inside the dilution refrigerator. The signals are sufficiently attenuated at each temperature stage of the cryostat to suppress thermal noise from the room-temperature part. The coaxial cables

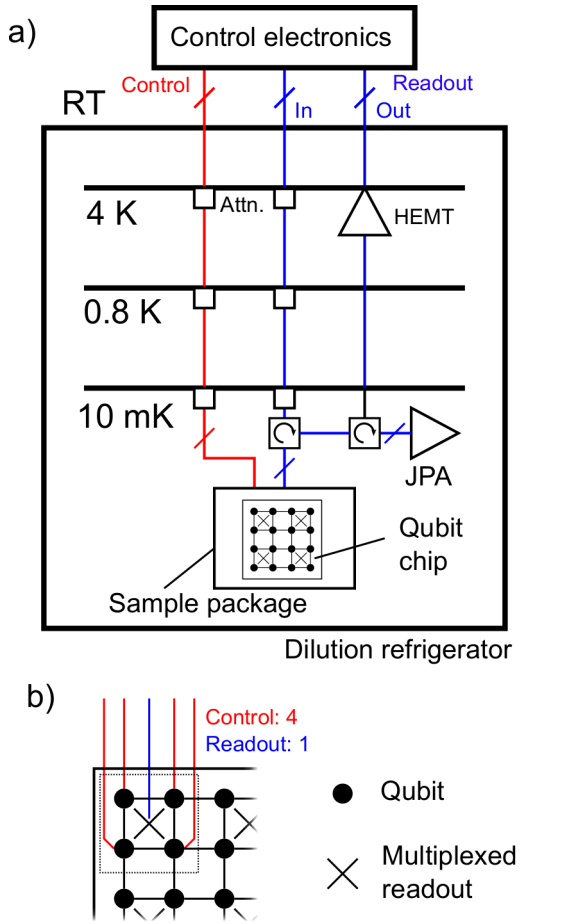

Fig. 2 (a) Microwave signaling in a dilution fridge. The control and readout microwave lines are connected from the room temperature electronics to the sample package through coaxial cables. (b) Wiring of the cables to the qubits on a chip. The readout lines are multiplexed to reduce the number of wires.

are finally connected to the qubit chip inside the sample package as shown at the bottom of the figure. The readout signals are reflected from the chip and amplified with a quantum-limited Josephson parametric amplifier (JPA) followed by a high electron mobility transistor (HEMT) amplifier at the 4-K stage. The sample package routes the signals from the array of coaxial cables to the qubits on a chip [Fig. 2(b)]. Out-of-plane wiring is indispensable to achieve wiring for a large-scale two-dimensional array of qubits.

3. Sample Packaging

The role of sample packaging is not only for the wiring. Another important role of the packaging is to limit electromagnetic modes at the proximity of the qubit chip and suppress the decoherence caused by a leakage through those spurious modes. At first, we review the possible impact of the spurious modes on the qubits. We also introduce the methods proposed so far to suppress the spurious modes with the package and chip structure. Then we will review the scalable designs enabling the wiring and packaging.

3.1 Spurious Modes

The first influence we have to consider from the spurious modes is the qubit energy decay induced by them. Suppose there is a lossy electromagnetic mode with the decay rate κ at the proximity of a qubit. It creates a loss channel from the qubit to the environment through the sprious mode. The energy decay of the qubit through such a mode is called Purcell effect. The decay rate of the qubit, Γ, by the Purcell effect is expressed as [18]

$$\Gamma = \left(\frac{g}{\Delta}\right)^2 \kappa, \tag{1}$$

where g is the coupling strength between the qubit and the spurious mode, and Δ is the detuning between their frequencies.

Even if the decay rate of the spurious mode is small, there might be dephasing of the qubit because of dispersive coupling to the spurious mode. The induced dephasing rate Γ_ϕ can be written as [22]

$$\Gamma_\phi = \frac{\chi_{\text{eff}}^2 \kappa}{(\kappa/2)^2 + \chi_{\text{eff}}^2} \bar{n}, \tag{2}$$

where χ_{eff} is the dispersive shift and $\bar{n}$ is the average photon number in the spurious mode. Equation (2) means that the residual thermal photons in the spurious mode contributes to the dephasing. Denoting the anharmonicity of the qubit as α, the dispersive shift can be written as $\chi_{\text{eff}} = g^2\alpha/[\Delta(\Delta+\alpha)]$ in the case of transmon [18]. There is also a frequency shift of the qubit, Δ_{ac}, because of the ac Stark shift [22]

$$\Delta_{\text{ac}} = \frac{\chi_{\text{eff}} \kappa^2/2}{(\kappa/2)^2 + \chi_{\text{eff}}^2} \bar{n}, \tag{3}$$

when there are thermal photons remaining in the spurious mode. It stresses the importance of thermalizing the chip through the sample package.

In the case when the spurious mode is coupled to multiple qubits or multiple control lines, the situation is even worse. The Purcell decay to the control lines can cause the crosstalk of the control microwave. Suppose the spurious mode couple to the i-th control line with the decay rate κ_i and j-th qubit with the coupling strength g_j, the i-th control line effectively coupled to the j-th qubit with the qubit decay rate

$$\Gamma_{\text{crosstalk}}^{(ji)} = \left(\frac{g_j}{\Delta_j}\right)^2 \kappa_i, \tag{4}$$

through the Purcell effect, where Δ_j is the detuning between the spurious mode and the j-th qubit.

The coupling of a spurious mode with multiple qubits also causes unnecessary interaction between qubits with the strength of

$$g_{ij} = \frac{g_i g_j}{\Delta_{ij}} \tag{5}$$

where $\Delta_{ij}^{-1} = (\Delta_i^{-1} + \Delta_i^{-1})/2$ [23], [24]. The unwanted interaction degrades the performance of the quantum gates. As it is hard to decouple all the spurious modes from the qubits, a more straightforward strategy is to detune the possible spurious mode from the qubits as much as possible.

One of the most harmful spurious modes is the so-called chip mode, which is the rectangular cavity mode standing in the substrate. Assuming that the dielectric constant of silicon to be $\epsilon_r = 11.45$ [25], the chip with the size $5 \times 5\,\text{mm}^2$ has a chip mode at 11.5 GHz. The chip mode can only be suppressed by inserting periodic metal structures with a spacing less than the target wavelength. Through-silicon vias (TSVs) [26]–[29] are one of the best ways to implement the metallic structure in a chip. Metallic pillar structures made by machining are also useful for this purpose [30]. A similar rectangular cavity mode can also exist in the housing surrounding the chip. This mode is called a box mode and has a relatively high frequency than the chip mode because of the dielectric constant of air $\epsilon_r = 1$. However, for a large chip size, we need to care about the box mode as well. A metallic cap structure bump-bonded to the qubit chip helps to suppress low-frequency box modes above a qubit chip by limiting the size of the box [31]. A bump-bonded interposer also serves similarly to suppress the box modes [32]. The difficulty of making those cap structures is that we have to avoid any additional dielectric loss. This prevents us from using conventional passivation layers on the silicon chip and forces us to stack the qubit chip and the cover chip without any dielectric layer. Another possible mode on a chip is a slot-line mode between separated ground planes. Air-bridges are often used to suppress the slot-line modes [33]. TSVs also connect divided ground planes through a backside ground and suppress the slot-line modes.

Once we design the packaging and chip structure that can reduce the number of the spurious modes, we have to confirm the frequencies of remaining spurious modes either numerically or experimentally. The eigenmode analysis with a periodic boundary condition helps to reveal the possible eigenmodes in the package in a scalable manner [30]. Even if we can find the eigenmodes in the electromagnetic simulation, it is difficult to know the residual coupling and the crosstalk through all the existing higher-frequency modes. The formulation using a circuit model is useful to analyze the net coupling and crosstalk in the package [34]. Especially, there is a method to estimate the residual coupling and crosstalk from simulated results of the impedance matrix between qubits and control lines [35].

There is also experimental method to evaluate these sprious modes. Two-tone spectroscopy of the package helps to characterize the hidden modes and their linewidths [36]. This method uses a qubit on the chip as a sensor and measure the dephasing of the qubit while sweeping the microwave drive for the spurious mode excitation. Coupling strengths between qubits and spurious modes can also be estimated by combining measurements of the dephasing and the ac Stark shift [37].

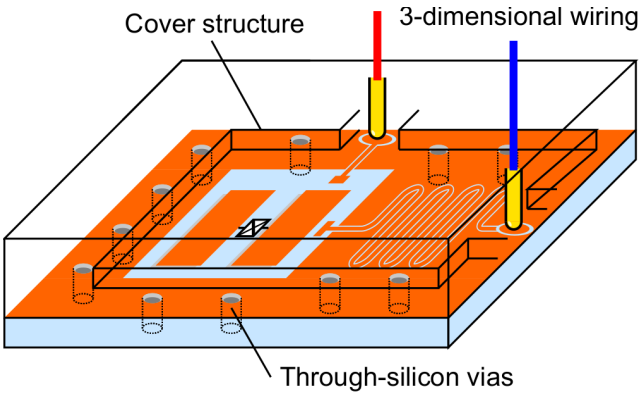

Fig. 3 An example of a required structure for large-scale packaging. The chip mode and the box mode need to be suppressed by the TSVs and the cover chip. The coaxial cables should be routed from the vertical direction.

3.2 Wiring and Integration

The packaging also needs to provide a wiring scheme. As the surface code requires a two-dimensional array of qubits, the control and readout lines should be connected from vertical directions. A schematic of a unit structure for large-scale packaging is shown in Fig. 3. Each qubit and resonator should be surrounded by TSVs and a cover structure to suppress both chip and box modes, while allowing vertical wiring. There are multiple ways of implementing three-dimensional wiring in the superconducting qubits. Flip-chip bonding of two chips is a common approach to separate the qubit chip and the chip for routing [38]. However, stacking two chips does not guarantee the scalability of the wiring, as the wiring is in the end made through the edges of the routing chip. To implement a fully scalable three-dimensional package, we need either a multi-layer stack of the routing chip [39] or to connect coaxial cables from the vertical direction [30], [40]. Spring probes are one of the possible methods of connecting the coaxial cables to the qubit chip directly [41], [42].

4. Future Developments

To scale up the number of qubits further, every related structure inside the fridge should be scalable. It includes the qubit chip, wiring, microwave components, and electronics. This means that the qubit chip should be composed of a repeated tileable pattern. It requires the uniformity of circuit parameters, especially those of the Josephson junctions. The trimming of junction inductance by laser-assisted annealing recently improved the uniformity significantly [43], [44]. Other than the uniformity, the size of a silicon wafer will limit the scalability at some point. The technique to interconnect the separated chips in a lateral direction would be required in such a scale [45].

The wiring inside the fridge (from room temperature to 10 mK) should also be integrated in a scalable manner. Currently wiring is done by using coaxial cables, but it would be difficult to install more than 1,000 lines in the same manner. Large-scale quantum computers would require the integration of wiring as well. High-density microwave signaling through microstrip transmission lines on a polyimide film might help to reduce the volume occupation in the fridge [46]. Further integration of the fridge wiring would require further multiplexing of the signals. Recently, the qubit control and readout through a photonic link were demonstrated toward multiplexing the microwave signals over an optical fiber [47].

Finally, the integration of control electronics is also an important future direction. Cryogenic electronics using single-flux-quantum (SFQ) circuits would be one of the energy-efficient ways for integrating the control electronics in a fridge [48]. Cryogenic CMOS circuits are also of great interest as a way to integrate not only waveform generating circuits but also their digital controller on the 4-K stage [49].

5. Conclusion

We have reviewed the packaging and wiring for a large-scale superconducting qubit chip. Suppression of the spurious modes and scalable implementation of the wiring are essential for large-scale packaging. We have addressed the required technologies to scale up the entire structure of the superconducting quantum computer. Continuous efforts to develop underlying technologies for integration are still necessary to realize fault-tolerant quantum computers.

Acknowledgments

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