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InP-Based Monolithic Photonic Integrated Devices

Liming ZHANG[†a)], **Christopher R. DOERR**[†], **Pietro BERNASCONI**[†], **Lawrence L. BUHL**[†], **Nicholas SAUER**[†], *and* **David T. NEILSON**[†], *Nonmembers*

SUMMARY We present our recent work on monolithically integrated devices comprising a variety of functional elements such as high speed optical transmitters and receivers, electro-absorption modulators integrated with tunable dispersion compensators and fast-tunable wavelength converters.

key words: *photonic integration, wavelength converter, high speed modulator and receiver, advanced modulation format*

1. Introduction

Photonic integration is an important path toward delivering optical modules with enhanced functionality at a reduced cost. Two approaches have been proposed: the parallel approach integrates arrays of the same elements, while the serial approach groups several different elements sitting along the path of an optical signal. Both cases generally aim at a size reduction, packaging and testing simplification, or lower power consumption. Provided the fabrication yield does not degrade to unacceptable levels, the functionality can be increased by combining passive and active or multiple active components on the same optical chip and, the cost per module may be drastically reduced by considerably simplifying the packaging requirements [1]–[3].

InP and its compounds are direct bandgap materials which make them ideal for many high performance optical components such as lasers, modulators and detectors. By inter-connecting these optical components with low loss InP passive waveguides, one can make multifunction integrated devices. In this paper, we review some of our recent works on monolithic photonic integrated circuits (PIC). The paper is organized as follows: in section two, we will present optical transmitters and receivers with speed up to 107 Gb/s. We demonstrate our integrated tunable dispersion compensator in section three. Section four will give an overview on an integrated 40 Gb/s wavelength converter. Finally, we will give a brief conclusion in section five.

2. High Speed Optical Transmitters and Receivers

The next generation Ethernet is likely to have a data rate of 100 Gb/s [4]. One possibility to accomplish 100 Gb/s transmission is to use many parallel low-speed channels. However the parallel approach has a low spectral efficiency, requires careful de-skewing, and has a large footprint or consumes significant chip real estate. Another possibility is to use one 100 Gb/s serial channel. With a multi-level modulation format, such as differential quadrature phase-shift keying (DQPSK), the serial approach has a high spectral efficiency and no de-skewing issues. A 100 Gb/s serial channel with a multi-level format may even work on existing 10 Gb/s dense wavelength-division multiplexed (DWDM) systems.

2.1 107 Gb/s DQPSK Receiver

The InP DQPSK receiver chip is shown in Fig. 1. The PIC integrated a delay interferometer (DI) and two pairs of high speed photodiodes (PDs) [5]. The DI consists of a 1×2 multi-mode interference (MMI) coupler; two waveguides with a differential delay of 18.7 ps, which is a one-symbol delay for 107-Gb/s DQPSK; and a 2×4 star coupler. The 2×4 star coupler serves as a 90° optical hybrid, allowing DQPSK demodulation with only one DI [6]. The waveguide cross sections for the passive waveguide, photodetector, and phase-shifter portions are depicted in Fig. 2. The waveguides are ridge waveguides with a benzocyclobutene (BCB) cladding. The PDs are 3 μm wide and 25 μm long.

The fabrication of the device is as follows [7]: First, a InP buffer layer, the guiding InGaAsP layer, the absorbing InGaAs layer, and a thin p:InP layer are grown onto a 2-inch n-doped InP wafer. The absorbing InGaAs layer is p-doped one third of the way through, resulting in a partially-depleted waveguide photodiode [8]. We then deposit silica, pattern it, and wet-etch off the p:InP and InGaAs everywhere except on top of the PDs. After that, we grow InP with a gradually increasing p-dopant concentration starting from a nominally undoped level. Then we remove the oxide and grow heavily p-doped InP and the InGaAs contact layer. We remove the InGaAs contact layer over the passive waveguides, and we etch 2 μm deep under where the PD bond pads would be, in order to reduce the pad capacitance. We etch the waveguides using reactive-ion etching to a depth of ~2 μm. We spin on BCB, etch openings over the phase shifter and PDs, and then deposit the contact metals. No anti-reflection coatings were applied for present demonstration.

The packaging of the PIC is as follows: two of the four PDs are wire-bonded to 50 Ω-terminated microstrip lines that connect to GPPO connectors. The termination con-

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[†]The authors are with Bell Labs, Alcatel-Lucent, 791 Holmdel-Keyport Rd, Holmdel, NJ 07733, USA.

a) E-mail: lmz@alcatel-lucent.com

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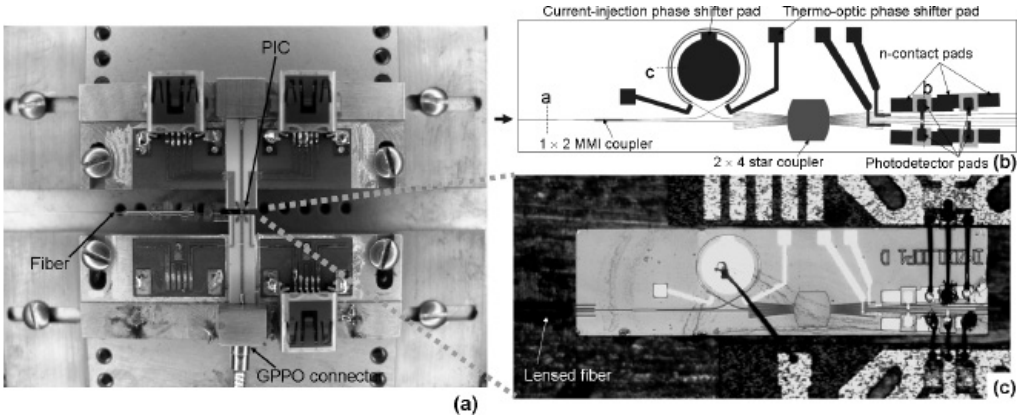

Fig. 1 DQPSK receiver PIC. (a) photograph of the packaged receiver, (b) waveguide layout, and (c) close-up photograph of the PIC. The PIC size is 3.2 mm × 0.8 mm.

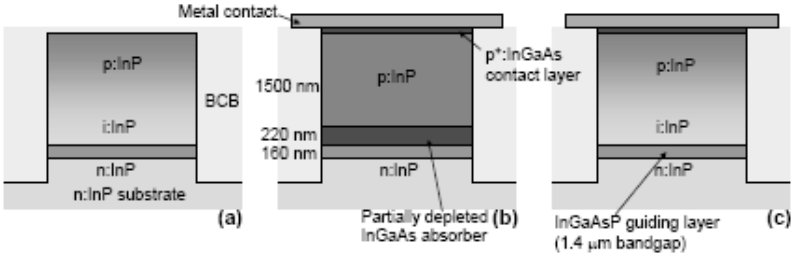

Fig. 2 Waveguide cross sections (see Fig. 1(b) for locations): (a) passive waveguide, (b) photodetector, (c) phase shifter.

sists of two parallel 100 Ω thin-film resistors on a BeO_3 substrate. Near the PIC, the microstrip line transitions to a grounded coplanar waveguide, where wire bonding to the PD is achieved in a manner similar to what is described in [9]. The phase shifter is wire bonded to a lead that connects to a universal serial bus connector.

We launched a 107 Gb/s return-to-zero DQPSK signal with a pre-coded pattern with a $2^{31}-1$ pseudo-random bit sequence (PRBS) at 188.6 THz (1589.6 nm) at +15 dBm into the receiver. The measured electrical eye diagram from one of the PDs with the phase shifter set to demodulate one of the quadratures is shown in Fig. 3. This signal was amplified by a 22-dB gain electrical amplifier. We observed an error floor at 6×10^{-4} bit error rate (BER).

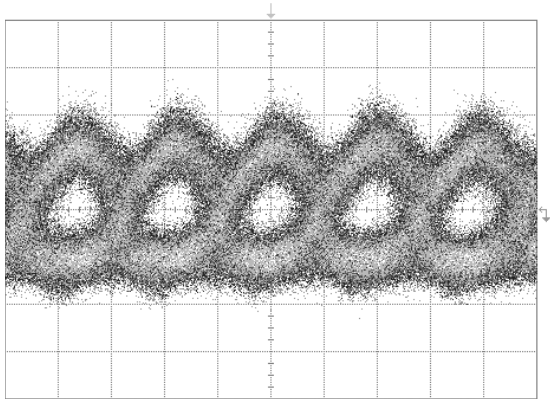

Fig. 3 A measured electrical eye diagram from the receiver (single-ended, one quadrature of 107-Gb/s DQPSK). (10 ps/div).

2.2 107 Gb/s DQPSK Transmitter

The integrated DQPSK modulator is shown in Fig. 4. The device consists of two electro-absorption modulators (EAMs) in a three-arm interferometer [10], [11]. The lower arm has a 90° phase relative to upper arm, and the center arm has a −135° phase difference from upper arm. The required power splitting ratio of each 1 × 3 coupler is 37%, 26%, 37%.

The modulator contains two EAMs and four static phase shifters [see Fig. 4(c)]. One static phase shifter is on the upper arm, one on the lower arm, and two on the center arm. The static phase shifters can be driven with a positive or negative voltage. With a negative voltage, the shifter also attenuates. The desired 1 × 3 coupler power splitting ratio is achieved by using a star coupler [12] with a narrower center waveguide inlet than the inlets of the outer waveguides, as shown in Fig. 4(d). The layer stack is shown in Fig. 4(b). The EAM is 115 μm long and 1.8 μm wide.

The device is considerably easier to fabricate compared to the DQPSK receiver. A 2 μm-thick n-doped InP layer is grown on a regular 2-in n-doped InP wafer, followed by 8 quantum wells (QWs) sandwiched between 10 nm of 1.3 μm-bandgap InGaAsP separate confinement layers, a

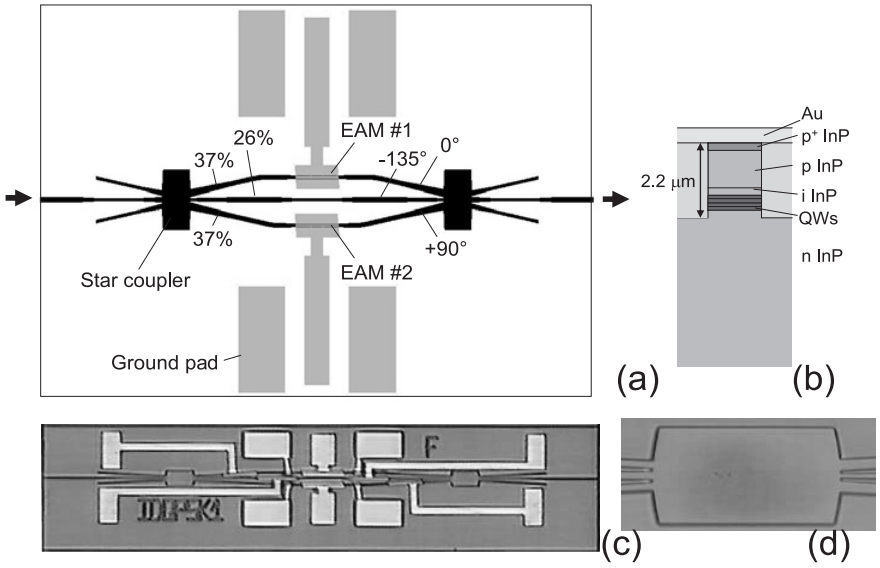

Fig. 4 (a) The schematic diagram of the DQPSK modulator. The static phase shifter metal pads are not shown. (b) Cross-section of the EAM. (c) Photograph of the chip. The chip size is $1500\,\mu\text{m} \times 250\,\mu\text{m}$. (d) Close-up photograph of the left-hand star coupler.

250 nm undoped InP layer, a $1.4\,\mu$m p-doped InP layer with gradually increased doping, and finally a heavily p-doped InGaAs layer. The passive waveguide has the same quantum wells structure as the modulator. This greatly simplified our fabrication as only one epitaxal growth was needed. The drawback of this approach is that the passive waveguide suffers higher loss.

The first processing step is removing the heavily p-doped InGaAs layer over the passive waveguides, mainly for electrical isolation. Then the waveguides are reactive-ion etched using silica as a mask to a depth of $2.2\,\mu$m. Benzocyclobutene (BCB) is then spun on and cured. Ground pads are etched through the BCB to the n-doped InP. Then small openings in the BCB are etched over the modulators and static phase shifters. The top-side metal is then deposited and patterned via lift-off. Finally, the wafer is thinned, and back-side metal is deposited.

The modulator was accessed optically via lensed fibers and electrically via two high-speed probes with internal 50-ohm termination and four single-needle DC probes. The band edge of the quantum wells (QWs) is at ~1540 nm. The core material of the waveguide uses a wavelength much shorter than the band edge where the loss is ~2 dB/mm. For the following experiments we launched a continuous wave (CW) wavelength of 1540 nm from an external cavity laser into the modulator.

To test the EAM performance at a high speed, we scratched out two waveguides in the three-arm interferometer and modulated the EAM in the remaining arm with 53.5-Gb/s data, multiplexed from four 13.375-Gb/s data streams. The optical eye diagram is shown as the upper inset in Fig. 5, demonstrating that the EAMs are capable of 53.5-Gb/s non-return-to-zero (NRZ) generation. We then drove both EAMs on a fully functional device with delayed and inverted copies

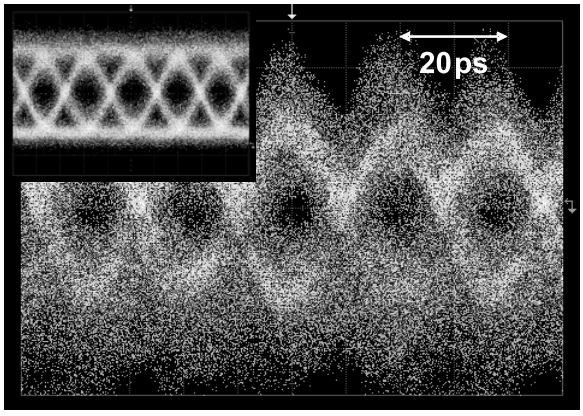

Fig. 5 107-Gb/s DQPSK eye diagram of one quadrature; upper inset is the 53.5-Gb/s NRZ eye diagram.

of the 53.5-Gb/s data stream. The demodulation is done by using a delayed Mach-Zehnder-interferometer silica photonic lightwave circuit. The eye diagram is shown in Fig. 5. The eye opening is small and tributary dependent. With a $2^7 - 1$ PRBS, the best tributary exhibited BER of $\sim 6 \times 10^{-4}$.

2.3 80 Gb/s Dual Polarization On-Off Key Modulator

Polarization-division multiplexing (PDM) can be used to double the transmission capacity in single-mode fiber [13]. A compact, monolithic, dual-polarization on-off-keying (DP-OOK) modulator PIC [14] is shown in Fig. 6. The device consists of two polarization beam splitters (PBS) and two polarization-independent electro-absorption modulators (EAMs). Each PBS consists of a 1×2 multimode interference (MMI) coupler, two identical waveguides with different path length, and a 2×2 MMI coupler. The first PBS

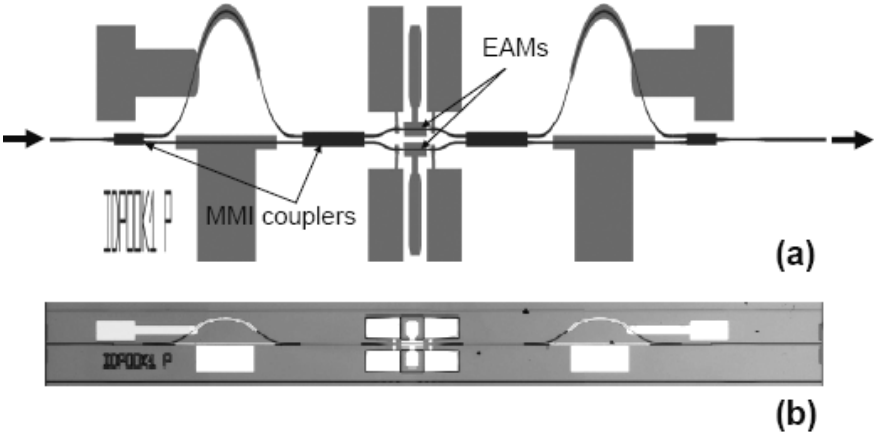

Fig. 6 (a) waveguide layout, stretched vertically for clarity; and (b) photograph of PIC. Size is 4 mm × 330 μm.

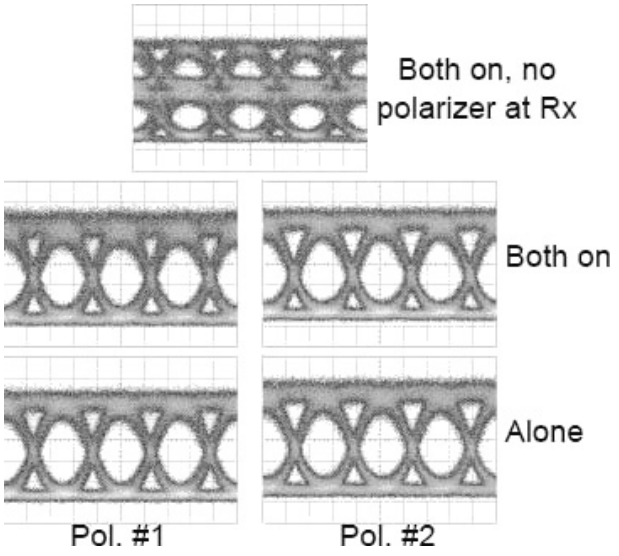

Fig. 7 Measured eye diagrams for the two polarizations, with and without simultaneous operation.

is used as a polarization splitter, the second one used as polarization combiner. The laser entered the device with equal power in both transverse electric (TE) and transverse magnetic (TM) polarizations, e.g. 45° polarized. The first PBS sends TE polarization to one EAM and TM to the other EAM, each driven with different data signals. The two signals are combined in the second PBS and exit the modulator. All the optical elements consist of 8 QWs in a p-i-n structure as in Fig. 2(b). The QWs are tensile strained to achieve a polarization-independent quantum-confined Stark effect.

The PIC was accessed optically via lensed fibers and electrically via two ground-signal-ground 50 Ω-terminated probes. The EAMs were driven with 40 Gb/s non-return-to-zero (NRZ) $2^{31} - 1$ PRBS, one inverted and delayed by 6 bits with respect to the other. The laser wavelength was 1543.5 nm. The launch power from the optical amplifier before the PIC was +13.5 dBm. Input polarization to the device was adjusted so that the powers in both polarizations exiting the device were equal. A polarizer was placed in front of the detector to demultiplex a channel. The eye diagrams for the two channels with and without simultaneous operation of the two channels are shown in Fig. 7.

3. 40 Gb/s Modulator Integrated with an Optical Tunable Dispersion Compensator

Optical transmission at baud rates ≥ 40-Gb/s requires an optical dispersion compensator (OTDC) for reaching distances larger than a few km. It is preferable that the dispersion compensator be adjustable. Optical tunable dispersion compensator (OTDC)s are still fairly bulky and power hungry. However, an OTDC can be combined with an electro-absorption modulator (EAM) into a compact monolithic chip with very low power consumption that may fit in a miniature transceiver [9]. As shown in Fig. 8(b), the EAM is followed by the OTDC in the form of a 3-arm asymmetric MZI consisting of two star couplers connected by passive guides with a linear path increment of 14.3 ps. Each arm is controlled by a phase and an amplitude adjuster in the form of a forward and reversed biased EAM, respectively.

The device is tested by modulating the EAM at 40 Gb/s (PRBS $2^{31} - 1$) and transmitting the NRZ signal over fibers with various dispersion amounts. The eye diagram is plotted in Fig. 9 with and without OTDC for the cases of −106 ps/nm, and +174 ps/nm. When the OTDC is not readjusted, the eye is closed at dispersion values of −106 ps/nm and +174 ps/nm. This is because the dispersion tolerance range for a 40 Gb/s NRZ signal with less than 1 dB penalty is only ∼80 ps/nm [15]. With optical equalization (OEQ) for dispersion, the dispersion tolerance range with less than 1 dB penalty increased to ∼280 ps/nm. The center of the dispersion tolerance range is positive because the EAM naturally produces a chirped signal with negative α. The total worst-case power consumption of the OEQ under all settings is less than 500 μW.

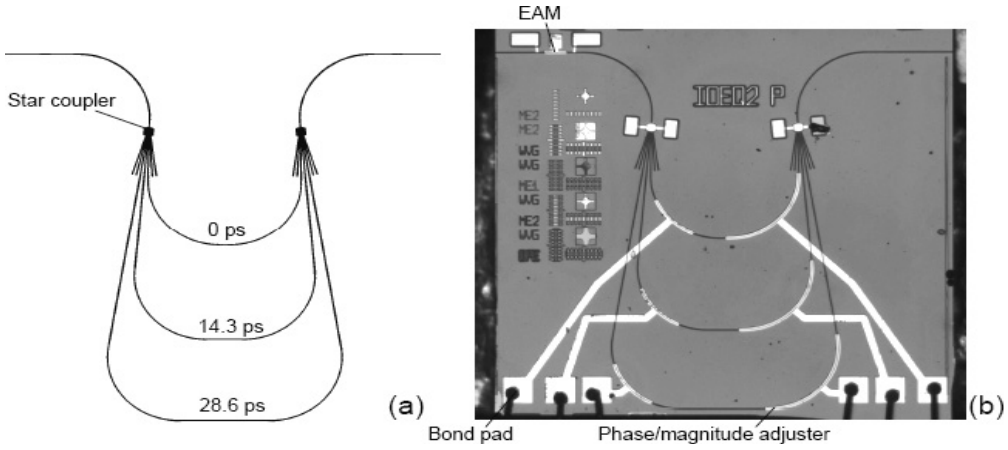

Fig. 8 EAM and OTDC. Size: $2.3 \times 2.2\,\mathrm{mm}^2$.

4. Fast Tunable Wavelength Converter Integrated with Tunable Laser

Wavelength conversion is a critical function in advanced wavelength division multiplexed (WDM) networks [16] and switching applications [17]. While wavelength conversion can be achieved using optical-to-electrical-to-optical (OEO) functionality, at higher data rates this becomes more challenging to implement compactly and at low power.

Our integrated wavelength-switch chip comprises a tunable CW laser source in the form of a multi-frequency laser (MFL) and a wavelength converter (WC) consisting of a semiconductor optical amplifier (SOA) followed by a delay filter [18], as shown in Fig. 10. The MFL is a multi-cavity oscillator that combines an array of 1 mm long SOA-based gain sections with a passive arrayed waveguide grating (AWG) as a wavelength dispersion element [19]. The grating is double-chirped both in length and in angle [20] to provide single-mode operation with high side-mode suppression ratios (SMSR). The wavelength is selected by driving current into one of the SOA's in the array. This kind of digital tuning makes the MFL very attractive for fast switching applications such as packet routing [21] since it can be tuned in less than a nanosecond. The current laser is designed to provide eight channels spaced by 100 GHz aligned around 1555 nm. Light is extracted from the cavity via a 3-dB coupler. The wavelength converter consists of a 2 mm long SOA as a non-linear element followed by an asymmetric MZI filter [22].

The chips are fabricated using a passive-active integration scheme that allows for monolithic integration of low-loss passive optical waveguides and SOAs. In contrast with the previous section, a buried rib-loaded waveguides are used as passive waveguides. The laser and SOA sections are buried in InP to improve heat dissipation. As described in detail in [19], the base wafers are grown by low-pressure metal organic chemical vapor deposition (MOCVD) and consist of a stack of a graded InGaAsP slab layers (λ_g = 1 μm to 1.3 μm), a 100-nm thick rib layer (λ_g = 1.3 μm), and

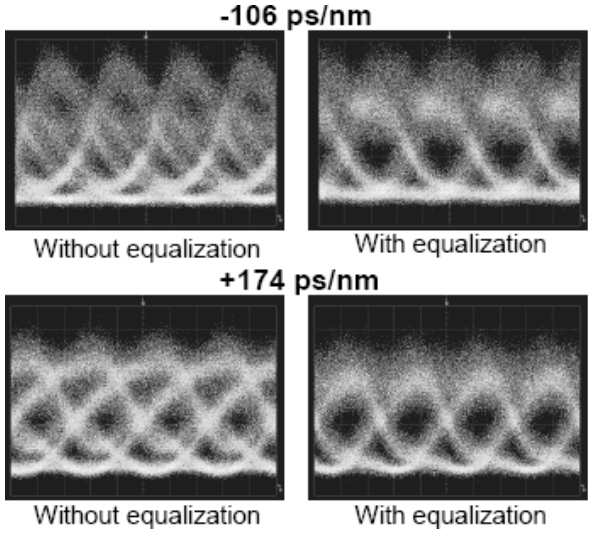

Fig. 9 40 Gb/s eye diagrams with and without OTDC.

an active layer with six tensile strained InGaAsP quantum-well layers separated by compressive strained (λ_g = 1.3 μm) barrier layers. In a first step, the active layer is removed everywhere except for the area occupied by the wavelength converter's SOA and the laser's gain sections. Then, the passive waveguides (arrayed waveguide grating, couplers, and access waveguides) and the SOA mesa are etched. This is followed by the overgrowth of a current blocking layer, an isolation step, a second overgrowth, and a metal deposition. The passive waveguides have a typical propagation loss as low as 0.2 dB/cm and a minimum waveguide bend radius of ~600 μm. The access waveguides at the facet are angled by 7° to suppress reflections while the laser cavity is formed by cleaved facets. No AR-coating had been applied at the time of characterization. The final device, 6.5 mm × 4 mm in size, was mounted on a thermoelectric cooler (TEC) and packaged with input and output lens fibers.

The MFL provides eight wavelengths spaced by 99.6 GHz around 1553 nm as shown in Fig. 11(a). There, the MZI filter is tuned via thermo-optic phase shifter so that the

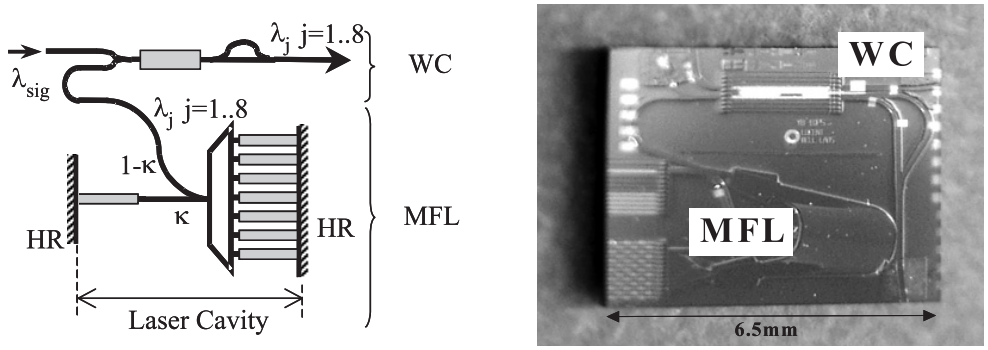

Fig. 10 Schematic (left) and picture (right) of monolithically integrated wavelength converter (SOA+MZI filter) and multi-frequency laser operating at 40 Gb/s line rates ($\kappa = 0.5$).

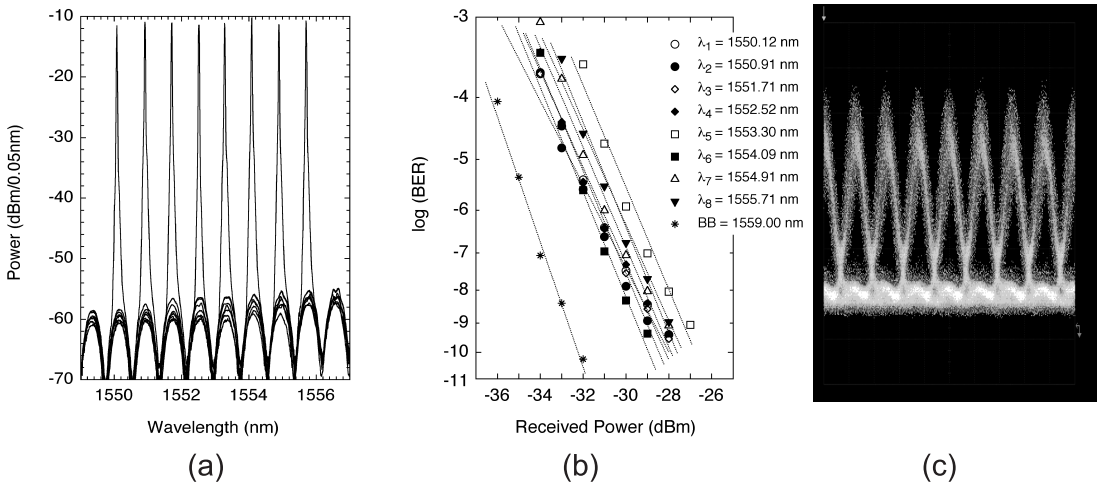

Fig. 11 (a) Overlapped spectra of the 8 MFL's wavelengths (b) BER measurements of eight converted 40 Gb/s signals (c) Example of 40 Gb/s wavelength converted eye diagram. (20 ps/div)

MFL's wavelengths sit at the transmission peaks of the filter. In an unpackaged device, laser with SMSR better than 35 dB is measured. The switching speed of the laser with proper electrical termination was measured to be sub-nanosecond. The measured 10–90% rise time was 270 ps and 90–10% fall time was 460 ps in an ON and OFF switching measurement with >13 dB extinction

The wavelength conversion performance of the device is evaluated through BER measurements. The signal source is a 40 Gb/s modulated RZ signal (PRBS $2^{15} - 1$) at 1559.0 nm with a pulse length of ∼3 ps. The signal is initially amplified by an EDFA and the amplified spontaneous emission is partially removed by a 3 nm wide filter. Input power and polarization are then adjusted before feeding the signal into the wavelength switch module. We estimate the required power on the chip to be of the order of 0 dBm. The 2 mm long wavelength converter SOA is pumped with 350 mA. The output wavelength is selected by switching the MFL's SOA and by fine tuning the output MZI filter via the thermo-optic phase shifter. The signals are pre-amplified, detected by an optical front-end with 30 GHz electrical bandwidth and coupled to a 40 Gb/s demultiplexer.

The results are summarized in Figs. 11(b) and 11(c). Error-free conversion is achieved for all eight converted channels with power penalties between 3 dB and 5.5 dB at BER = 10^{-9}. A better performance is expected when using a narrower filter before the receiver and by reducing the coupling losses at the device's output, so as to improve the received optical signal to noise ration.

It is worth noting that the integrated wavelength switch module may not require optical isolators to prevent back-reflection from reaching the MFL and destabilizing the laser operation. In fact, thanks to the MFL's geometry, any back-reflection outside the laser's channel bandwidth is automatically filtered by the AWG and absorbed by the inactive SOA's. In-band reflections do not seem to generate instabilities either. This remarkable property will facilitate the integration of laser sources into monolithic chips containing more and diversified functionalities and allowing for large-scale optical integration.

5. Conclusions

Recent work on our monolithic integrated photonic devices has been reviewed. A compact DQPSK transmitter and receiver were presented and both were shown to have poten-

tial to operate at 107 Gb/s. A novel DP-OOK modulator with a simple and robust design has been demonstrated, and shown its performance at 80 Gb/s. An EAM modulator with TODC has been integrated into a single chip. The integrated devices expanded the dispersion tolerance range from ~80 to ~280 ps/nm. Finally, a monolithic integration of wavelength converter and a rapidly tunable laser to construct a wavelength-switching element has been demonstrated. The device has been shown to operate at 40 Gb/s with ~0.5 ns wavelength switching times.

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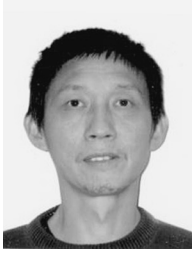

Liming Zhang received B.S. and M.S. degrees from physics department, USTC and Institute of Acoustics, China respectively. He obtained his Ph.D. degree in electrical engineering from University of Strathclyde in 1990, U.K. From 1990 to 1993, he was a Research Associate at Cambridge University, U.K., where he was engaged on theoretical study of long-wavelength distributed feedback lasers. He joined Bell Laboratories, Murray Hill, NJ, as a Member of Technical Staff in 1993, where he has designed high linearity analog lasers for CATV application and electro-absorptive modulator lasers for optical transmission systems. In 2001, he moved to Bell Laboratories, Crawford Hill Laboratory, Holmdel, NJ. His current research interest include MOCVD growth of III-V compound semiconductor materials, quantum dots emission at 1.55 μm, nonlinear application of semiconductor optical amplifiers, high-speed InP-based transceiver, and large scale photonic integration.

Christopher R. Doerr earned a B.S. in aeronautical engineering and a B.S., M.S., and Ph.D. in electrical engineering from the Massachusetts Institute of Technology (MIT). He attended MIT on an Air Force scholarship and earned pilot wings in 1991. Since coming to Bell Labs in 1995, Doerr's research has focused on integrated devices for optical communication. He was promoted to Distinguished Member of Technical Staff in 2000, received the OSA Engineering Excellence Award in 2002, and became an IEEE Fellow in 2006 and an OSA Fellow in 2009. Doerr was Editor-in-Chief of IEEE Photonics Technology Letters from 2007–2009. He is currently an Associate Editor for the Journal of Lightwave Technology. He is married to Neriko Musha and has two children.

Pietro Bernasconi received the Dipl. Phys. and Ph.D. degrees in Physics from the Swiss Federal Institute of Technology of Zurich, Institute of Quantum Electronics, in 1993 and 1998, respectively. In 1999 he joined Bell Laboratories of Alcatel-Lucent, Holmdel NJ, where he has been investigating photonic integrated circuits in Silicon bench technologies as well as in III-V semiconductor material structures for applications in optical communication systems.

Lawrence L. Buhl (Larry) first served in the US Army, Signal Corp, Fort Monmouth, NJ as an instructor, teaching Microwave theory and Radar systems. He joined Bell Laboratories in 1972, beginning early research work in metal vapor laser spectroscopy. In 1978, he began pioneering and developed various guided wave optical devices in $LiNbO_3$ and later, III-V materials. He received a B.Sc. in Electronic Engineering from Monmouth University in 1984. Since 2000, he has been investigating 10G and 40G systems and devices and recently assumed responsibility for optical and high speed device packaging.

Nick Sauer received his B.S. in physics and chemistry from Albany State University in 1984. He received his M.S. in physics and metallurgy from Stevens Institute of Technology. Since 1985 he has worked at Bell Laboratories on growing, characterizing and, most recently, processing of InP based optoelectronic devices.

David T. Neilson received the B.Sc. (Hons) degree in physics from Heriot-Watt University, Edinburgh, Scotland, in 1990 and the Ph.D. degree in physics for work on optical nonlinearities in InGaAs Quantum well devices from Heriot-Watt University in 1993. He was a Postdoctoral Researcher at Heriot-Watt University from 1993 to 1996,working on systems and devices for free space optical interconnects and switching. From 1996 to 1998, he was a Visiting Scientist at NEC Research Institute, Princeton, NJ, researching optical interconnects for high-performance computing. In 1998, he joined Bell Laboratories, Holmdel, NJ, where he has worked on MEMS based crossconnects, wavelength selective switches, equalizers, and dispersion compensators. He is currently a Technical Manager leading a group conducting research of highly integrated InP based optoelectronic components and subsystems and with responsibility for optoelectronic device growth and fabrication facility. His research interests also include role of optical interconnects and switching for high capacity optical switches and routers. He has over 130 publications and 20 issued patents in the field of optical interconnects, switching and optoelectronic devices. Dr. Neilson is a Senior Member of IEEE Photonics Society.