FOREWORD

Special Section on Multiple-Valued Logic and VLSI Computing

Recent development of high-functionality, compactness, low-energy consumption in System-on-Chip technology has been accelerated by device geometry reduction, however, serious problems not solved only by the geometry reduction have been becoming prominent. For the problem, innovative new-concept VLSI computing technology such as multiple-valued VLSI computing is strongly expected to be developed. Also, multiple-valued logic and algebra are expected to be effectively employed for logic design and verification. From this point of view, we have planned Special Section on Multiple-Valued Logic and VLSI Computing.

To discuss the same frontier area, the 39th IEEE International Symposium on Multiple-Valued Logic (ISMVL'09) was held on May 21–23, 2009 in Okinawa. We solicited for submission of the papers on multiple-valued logic and VLSI computing, not limited to the papers presented in ISMVL'09.

I hope the topics included in the Special Section will demonstrate recent development of novel and new-concept computing technology. Fourteen papers including two invited ones are accepted in the Special Issue which contents are divided into three subfields: logic design, multiple-valued circuit technology, and applications of multiple-valued VLSI.

The Guest Editor-in-Chief sincerely expresses appreciation to the following editorial committee members for their efforts in publishing this special issue. I also thank all the reviewers for their hard work.

Michitaka Kameyama, Guest Editor-in-Chief

Michitaka Kameyama *(Fellow)* received the B.E., M.E. and D.E. degrees in Electronic Engineering from Tohoku University, Sendai, Japan, in 1973, 1975, and 1978, respectively. He is currently a Dean and a Professor in the Graduate School of Information Sciences, Tohoku University. His general research interests are intelligent integrated systems for real-world applications, advanced VLSI architecture, and new-concept VLSI including multiple-valued VLSI computing. He received the Outstanding Paper Awards at the 1984, 1985, 1987 and 1989 IEEE International Symposiums on Multiple-Valued Logic, the Technically Excellent Award from the Society of Instrument and Control Engineers of Japan in 1986, the Outstanding Transactions Paper Award from the IEICE in 1989, the Technically Excellent Award from the Robotics Society of Japan in 1990, and the Special Award at the 9th LSI Design of the Year in 2002. He is an IEEE Fellow.